ABSTRACT OF THE DISCLOSURE

A layout design apparatus can develop a semiconductor integrated circuit in a shorter period at a lower cost. It includes an initial layout section for performing placement and routing using a netlist of the entire semiconductor integrated circuit such that a first circuit layout whose wiring consists of n ($n \geqq 2$) wiring layers is formed in a first circuit region, and a second circuit layout, which has wiring consisting of (n-m) ($m<n$) wiring layers and is connected to the first circuit layout, is formed in a second circuit region; and a layout modifying section for performing placement and routing using a netlist of a third circuit to form a third circuit layout such that its wiring consists of the (n-m) wiring layers constituting the wiring of the second circuit, and for replacing the second circuit layout by the third circuit layout.